claim 5 under 35 U.S.C. § 103(a) as unpatentable over Rhee, Teramoto, Komori and Hsu as applied to claim 1, and further in view of Takemura (U.S. Patent No. 5,917,221); and repeated the rejection of claim 7 under 35 U.S.C. § 103(a) as unpatentable over Rhee, Teramoto, Komori, Hsu, and Takemura as applied to claim 5, and further in view of Tomita, et al. (U.S. Patent No. 5,959,329).

Applicants respectfully traverse the rejections of claims 1 – 3, 5, and 7, as detailed above, for the following reasons. Applicants respectfully disagree with the Examiner's arguments and conclusions, and submit that a *prima facie* case of obviousness has not been established.

In order to establish a *prima facie* case of obviousness, three basic criteria must be met. First, the prior art reference (or references when combined) must teach or suggest all the claim elements. Second, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify a reference or to combine reference teachings. Third, there must be a reasonable expectation of success. *See* M.P.E.P. § 2143, 8th Ed., Aug. 2001, pp. 2100-122 – 127.

The Examiner does not show that all the elements of Applicants' claims are met in the cited references, taken alone or in combination, does not show that there is any suggestion or motivation to modify the cited references to result in the claimed invention, and does not show there would be any reasonable expectation of success from so doing.

Applicants' independent claim 1 recites, *inter alia*, a magnitude relationship between the nitrogen concentration of the gate insulating film and that of the post oxide film, vis-à-vis "a gate insulating film formed on the first region" and "a post oxide film formed on the second region." Thus, claim 1 recites a distribution of nitrogen concentration in a film containing the gate insulating film and the post oxide film, in the direction perpendicular to the thickness direction of

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the film, i.e., a horizontal distribution of nitrogen concentration, claimed: "a nitrogen concentration of the post oxide film is lower than that of the gate insulation film" (For illustrative and exemplary purposes only, please see attached "Reference Fig. 1" in the Appendix.)

The Examiner stated that Teramoto teaches a gate insulating film made of $SiO_xN_y$ that has the same nitrogen concentration distribution as that of the present invention. *See* Final Office Action, pp. 5 – 6. Applicants respectfully disagree with the Examiner's allegation.

As the Examiner correctly pointed out, Teramoto's Abstract and the composite figure contained on the patent cover page disclose a distribution of nitrogen concentration in the gate insulating layer. However, Teramoto's Abstract also discloses a nitrogen concentration distribution in the thickness direction of the gate insulating layer, i.e., a vertical distribution of nitrogen concentration (*See* attached "Reference Fig. 2" in the Appendix), which is different from the features recited in Applicants' claim 1. In the case of Teramoto, for one of reasonable skill in the art, it is reasonable to conclude that the nitrogen concentrations in the gate insulating layer are constant in the horizontal direction.

While Teramoto discloses a distribution of nitrogen concentration in the gate insulating layer, as mentioned above, it fails to disclose a distribution of nitrogen concentration in a post oxide film. Since Teramoto discloses a distribution of nitrogen concentration in the gate insulating layer in the thickness direction thereof, if the distribution of nitrogen concentration disclosed in Teramoto is applied to Rhee's oxide film 80 (which the Examiner applies to the post oxide film of the present invention), the oxide film 80 will have nitrogen concentrations that vary in the *thickness direction* thereof.

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Therefore, even if the nitrogen concentration distribution disclosed in Teramoto were applied to Rhee's oxide film 80 and the gate insulating film 60, the element of claim 1 "wherein a nitrogen concentration of the post oxide film is lower than that of the gate insulation film" cannot be derived therefrom. One skilled in the art would only arrive at the present claimed invention by consulting Applicants' disclosure. Therefore, the only way to construct the claimed invention from the cited references would be to rely on aspects related to the present invention. Such reliance, however, would constitute improper hindsight reasoning. "The mere fact that references can be combined or modified does not render the resultant combination obvious unless the prior art also suggests the desirability of the combination." M.P.E.P. § 2143.01, p. 2100-124, citing *In re Mills*, 16 USPQ2d 1430 (Fed. Cir. 1990).

The semiconductor device recited in Applicants' claim 1 uses "a post oxide film" having "a nitrogen concentration ... lower than that of the gate insulation film." In other words, the nitrogen concentration of the post oxide film is intentionally made lower to reduce the amount of current leaking in the gate edge portion.

In contrast, Teramoto fails to disclose an insulating layer having an intentionally lowered nitrogen concentration, though it discloses an $SiO_xN_y$ layer used as an insulating film, or, more specifically, a gate insulating film (in other words, the use of a silicon oxide layer with an intentionally *increased* nitrogen concentration).

One of the reasons that the nitrogen concentration of Teramoto's $SiO_xN_y$ layer peaks in the interface between the $SiO_xN_y$ layer and the gate electrode is to prevent the diffusion of impurities present in the gate electrode into the $SiO_xN_y$ layer (*See* Teramoto's Abstract). In other words, the nitrogen concentration of the $SiO_xN_y$ layer peaks at a predetermined place which different from that constructed according to Applicants' claimed invention.

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Therefore, even if Rhee and Teramoto are combined, a person skilled in the art cannot derive from their combination the semiconductor device recited in Applicants' claim 1, that is, by intentionally making the nitrogen concentration of the post oxide film lower, the amount of current leaking in the gate edge portion can be reduced.

The other cited references (Komori, Hsu, Takemura, and Tomita) also neither disclose nor suggest at least the above-described element of Applicants' claim 1, "wherein a nitrogen concentration of the post oxide film is lower than that of the gate insulation film" or the above-mentioned advantages. Therefore, Applicants submit that the 35 U.S.C. § 103(a) rejection of claims 1 – 3, 5, and 7 is improper and should be withdrawn.

Furthermore, Applicants submit the attached illustrative and exemplary "Reference Fig. 3" in the Appendix to facilitate a discussion with the Examiner regarding his rejection of Applicants' claims. In Reference Fig. 3, "sub" denotes the semiconductor substrate (e.g., it is an Si substrate), "C(PO)" denotes a capacitor comprising a gate electrode, a post oxide film and a semiconductor substrate, "C(SiON)" denotes a capacitor comprising a gate electrode, a gate insulating film and an Si substrate, "ε(Si)" denotes the permittivity of the Si substrate (not shown), "ε(PO)" denotes the permittivity of the post oxide film, "ε(SiON)" denotes the permittivity of the gate insulating film, "d(PO)" denotes the thickness of the post oxide film, "d(SiON)" denotes the thickness of the gate insulating film, and "Vg" denotes the gate voltage.

The relationship between the electric field, E1(sub), in the vertical direction in the surface of the Si substrate under the gate insulating film and the electric field, E(SiON), in the vertical direction in the gate insulating film can be expressed by the following equation (1):

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$$E1(sub) = \varepsilon(SiON) \cdot E(SiON)/\varepsilon(Si)$$

$$= \varepsilon(SiON) \cdot (Vg/d(SiON)/\varepsilon(Si) \quad \ldots(1)$$

The relationship between the electric field, E2(sub), in the vertical direction in the surface of the Si substrate under the post oxide film and the electric field, E(PO), in the vertical direction in the post oxide film can be expressed by the following equation (2):

$$E2(sub) = \varepsilon(PO) \cdot E(PO)/ \varepsilon(Si)$$

$$= \varepsilon(PO) \cdot (Vg/d(PO)/ \varepsilon(Si) \quad \ldots(2)$$

$\varepsilon(Si)$ takes the same value in both equations (1) and (2). Vg also takes the same value in both equations (1) and (2). Therefore, E2(sub) can be made smaller than E1(sub) by either making d(PO) thicker than d(SiON), or making $\varepsilon(PO)$ smaller than $\varepsilon(SiON)$. In other words, by intentionally making the nitrogen concentration of the post oxide film lower, $\varepsilon(PO)$ is made smaller than $\varepsilon(SiON)$, and the electric field, E2(sub), in the vertical direction in the surface of the Si substrate under the post oxide film, is made lower.

Applicants submit two more reference Figures in the attached Appendix to facilitate discussion with the Examiner: Reference Fig. 4A shows a post-oxide film with a low nitrogen concentration/Si-substrate band diagram, and Reference Fig. 4B shows a gate-insulating film with a high nitrogen concentration/Si-substrate band diagram. Each of Reference Figs. 4A and 4B shows a band diagram in the case where the post oxide film and the gate insulating film have the same thickness.

As shown in Reference Figs. 4A and 4B, the strength of the electric field, E2, in the vertical direction in the surface of the Si substrate under the post oxide film, and the strength of the electric field, E1, in the vertical direction in the surface of the Si substrate under the gate

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insulating film, are *different*, and therefore, the potential barrier felt by the electrons "e⁻" in one Si substrate surface, and the potential barrier felt by electrons "e⁻" in the other Si substrate surface, are *different*. This is because when the electric field in the vertical direction is high, the Fermi level of the Si substrate surface increases (by quantum effects). As a result, the tunneling probability of electrons "e⁻" becomes lower in the gate edge portion with a lower nitrogen concentration where the electric field in the vertical direction of the Si substrate surface is lower, and the amount of leak current is reduced in the gate edge portion. The above-described advantage is neither taught nor suggested by any of the cited references (Rhee, Teramoto, Komori, Hsu, and Takemura), taken alone or in combination.

Therefore, by the reasons just argued, Applicants have demonstrated the patentability of Applicants' independent claim 1. The addition of other references, in the rejections of dependent claims 5 and 7, respectively, still does not cure the deficiencies of Rhee, Teramoto, Komori, and Hsu as applied to Applicants' independent claim 1, in that they still do not address the features of Applicants' present invention not taught or suggested by Rhee, Teramoto, Komori, and Hsu. Therefore, Applicants submit that dependent claims 2, 3, 5, and 7 are also allowable at least by virtue of their dependence from allowable base claim 1.

**Conclusion:**

In making various references to the specification and drawings set forth herein and in the attached Figure references, it is understood that Applicants are in no way intending to limit the scope of the claims to the exemplary embodiments described in the specification and illustrated in the drawings. Rather, Applicants expressly affirm that they are entitled to have the claims interpreted broadly, to the maximum extent permitted by statute, regulation, and applicable case law.

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In view of the foregoing, Applicants request the Examiner's reconsideration of the application and submit that the rejections detailed above are improper and should be withdrawn. Applicants submit that independent claim 1 is in condition for allowance as are dependent claims 2, 3, 5, and 7. Applicants therefore request the Examiner's reconsideration of the application, and the timely allowance of the pending claims.

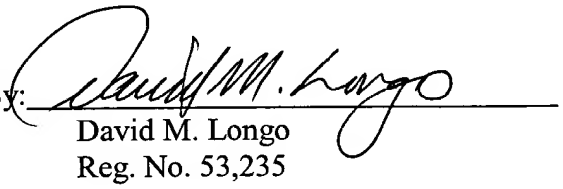
Should the Examiner continue to dispute the patentability of the claims after consideration of this Request, Applicants encourage the Examiner to contact Applicants' undersigned representative by telephone to discuss any remaining issues or to resolve any misunderstandings.

Please grant any extensions of time under 37 C.F.R. § 1.136 required in entering this response. If there are any fees due under 37 C.F.R. § 1.16 or 1.17, which are not enclosed, including any fees required for an extension of time under 37 C.F.R. § 1.136, please charge such fees to our deposit account 06-0916.

Respectfully submitted,

FINNEGAN, HENDERSON, FARABOW,
GARRETT & DUNNER, L.L.P.

Dated: March 3, 2003

By: 
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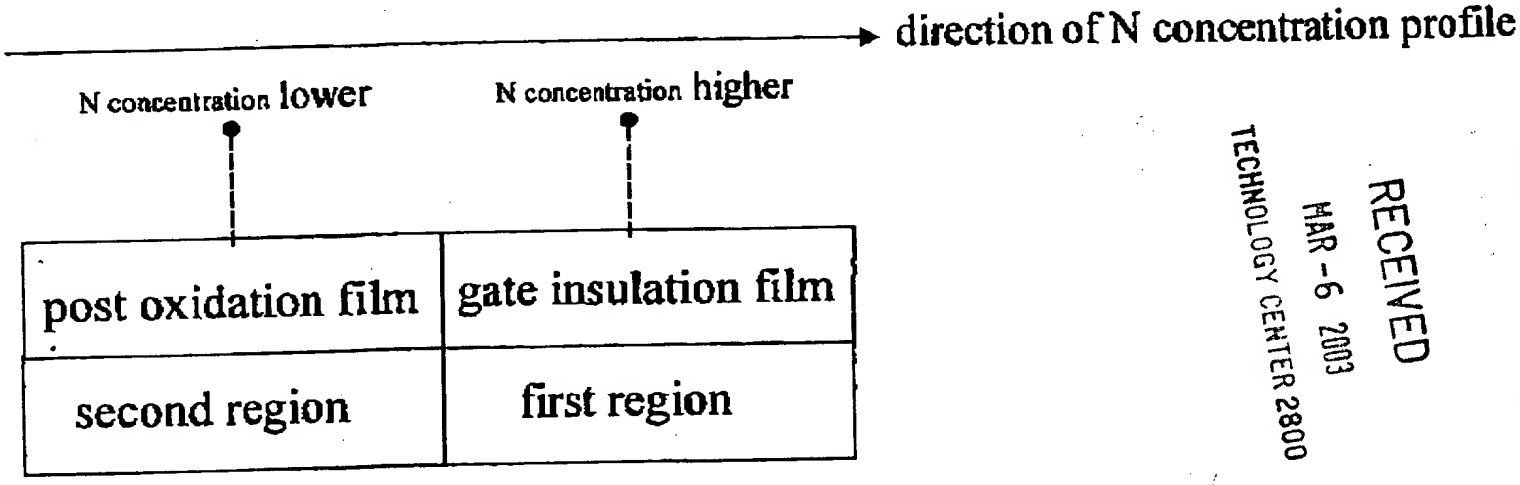
Application Number: 09/559,757
Filing Date: April 27, 2000
Attorney Docket Number: 04329.2306

**APPENDIX TO REQUEST FOR RECONSIDERATION AFTER FINAL**

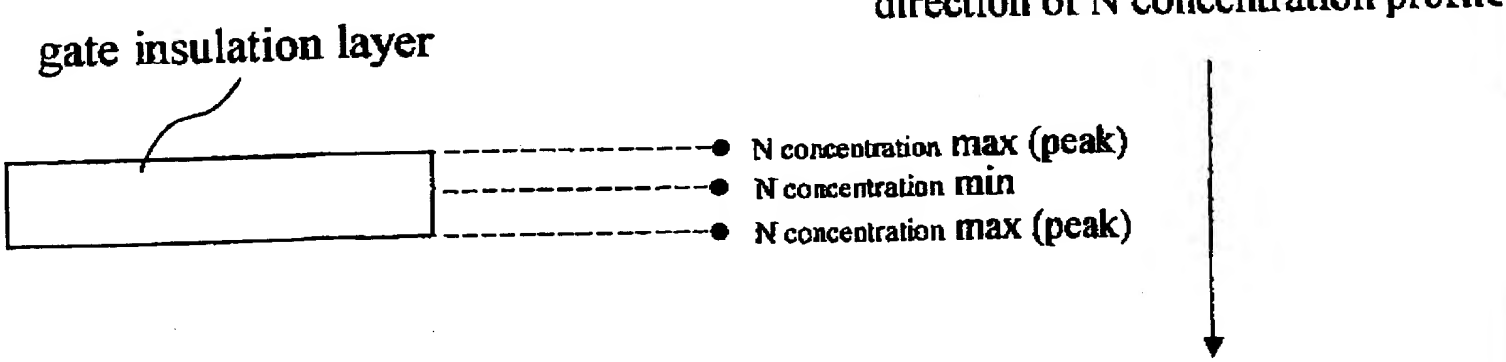
**"REFERENCE FIGURES"**

# REFERENCE FIG.1

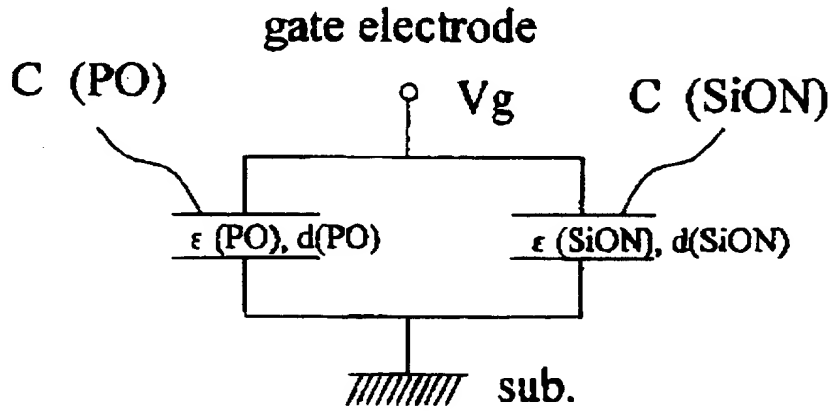




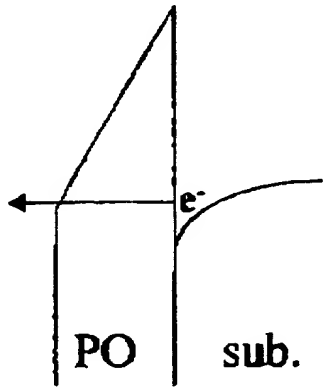

# reference fig.2 (Teramoto)



# REFERENCE FIG.3

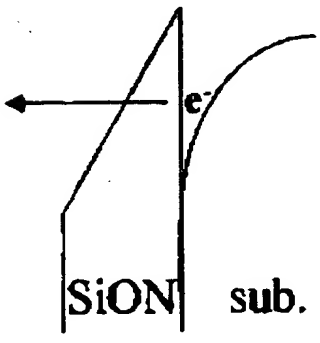


# REFERENCE FIG.4A




low E2(sub.)
(N concentration lower )

# REFERENCE FIG.4B




high E1(sub.)
(N concentration higher )